FREQUENCY MEASUREMENT FOR USE WITH A MICROPROCESSOR-BASED WATER TURBINE GOVERNOR

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I INTRODUCTION

One of the most important indices of the quality of electrical energy is frequency. Its measurement plays a fundamental role in the regulation performance. In the specification of the hydro turbine control system (Fig. 1), there are three indices which are directly related to the speed/frequency measurement [1,2]:

(i) Speed fluctuation for no-load operation must be equal to or less than 20.16%.
(ii) Speed dead-band (1k) must be smaller than 0.02%.
(iii) Dead-time of main servo-motor for the rejections of 210% load (Tq) must be smaller than 0.2 s.

According to the indices listed above and considering the dead-band of the servo-mechanical mechanism, the resolution of the speed/frequency measurement must be less than 0.05%. Also, the response speed should be less than 0.2 s. In addition, the speed/frequency measurement should have wide ranges for improving start-up, shut-down and load rejection performance.

The conventional measurement techniques can hardly meet all these requirements at one time. In the last decade, microprocessor based techniques have appeared as strong rivals in both control and measurement applications and the conventional speed/frequency measurement is being replaced by digital means.

Generally, speed signal has been employed in the speed governors [3,4]. Many good digital techniques to measure speed have been developed [5,6,7]. In speed measurement, a special purpose sensor, such as an optical disc, a magnetic pickup or a tacho generator, has to be installed on the generating unit’s rotor [5,7]. It rotates with the rotor and converts a speed signal to an electrical signal for the digital measuring device. The quality of performance of the transducer is largely due to the high performance of digital techniques. The cost of a good transducer is usually high. Moreover, the parameters used in the measurement transducer have to be changed to match the speed of each individual installation. This can make the field installation inconvenient.

Many purely digital frequency measurement techniques for electric power systems have been proposed [8,9,10,11]. However, most of them are designed for pure measurement or protection purposes, and are generally not suited to meet the special demands of governor application.

A digital frequency measurement approach specially designed for the speed governors is proposed in this paper. This approach has been successfully applied to 12 speed governors for water turbines (includes II governors installed in 7 hydro power stations [12]) since 1994 when the first microprocessor-based governor was put into operation in Ouyanghai hydro power station in China. Test results [12] of all these governors have shown that this frequency measurement approach can very well meet the requirement of speed control in electric power systems.

This approach has also been adopted in the research prototype of a highly reliable fault-tolerant water turbine governor jointly developed by the department of electrical engineering, the University of Calgary, and the department of electrical engineering, Huazhong University of Science and Technology [12,13,14]. This research prototype is planned to be tested in a hydro power station in June 1990. The frequency measurement principle is presented in section 2. The hardware and the software implementation of frequency measurement integrated into this research prototype are described in section 3 and section 4 respectively. The performance and test results are presented in section 5.

II PRINCIPLE OF FREQUENCY MEASUREMENT

As is well known, the timing characteristic of an alternating signal can be described either in frequency (f) or by period (T). From the viewpoint of digital measurement, the frequency and the period can be defined as below: 

Definition 1: The frequency of an alternating signal is the number of times the signal crosses zero level from
negative to positive (or from positive to negative) in a unit time (e.g., per second).

**Definition 2:** The period of an alternating signal is the time the signal takes from one zero-level crossing to the next zero-level crossing in the same direction.

The period is inversely proportional to the frequency. Obviously, the frequency of an alternating signal can be obtained in two ways based on the two definitions above:

1) Counting the number of times of zero-level crossing in the same direction in a unit time. The frequency, \( f \), equals this number.
2) Measuring the time, \( T \), from one zero-level crossing to the next zero-level crossing in the same direction. The frequency is then equal to \( 1/T \).

The first method is ideal for measuring high frequency with slow change. Generally, the second method is more suitable for low frequency. The frequency of electric power systems is low. Moreover, its change in two consecutive cycles can be relatively fast. Therefore, the second method is more suitable for this application [8]. Basically, the idea is to use one crossing of zero level from negative to positive (or from positive to negative) to start a “stopwatch” and to use the next zero-crossing in the same direction to stop the “stopwatch”, and so on. The time shown on the “stopwatch” is the period \( T \). Then \( f \) equals \( 1/T \).

The principle of this frequency measurement approach is shown in Fig. 2. A voltage comparator is used to shape the alternating signal to a logic signal (square wave). Then the frequency is divided by 2. The true output of the divider is connected to the control input of the timer (this control input is called gate input). The frequency with slow change can be relatively fast. Therefore, the second method is more suitable for this application.

The frequency of an alternating signal is the number of times of zero-level crossing in the same direction in a unit time (e.g., per second). The frequency, \( f \), is divided by 2. The frequency is then equal to \( 1/T \). With microprocessors, this conversion is very simple.

The principle of this frequency measurement approach is shown in Fig. 2. A voltage comparator is used to shape the alternating signal to a logic signal (square wave). Then the frequency is divided by 2. The true output of the divider is connected to the control input of the timer (this control input is called gate input). The frequency with slow change can be relatively fast. Therefore, the second method is more suitable for this application.

The false output of the D flip-flop (point 5 in Fig. 3) is connected to the interrupt controller (Intel 8259). The false output of the D flip-flop happens at the same time as the rising edge of the false output of the same D flip-flop. The microprocessor is interrupted at point 7 in Fig. 3) as soon as the timer is stopped. The microprocessor picks up the timing result and reloads the timer, and so on.

The principle used in this paper (Fig. 3) is connected to the interrupt controller. When the timer overflows, the microprocessor adds 1 to an extending counter in RAM and reloads the timer. In this way, the lowest frequency which can be measured by this circuitry mainly depends on the voltage output of the generator, e.g. if the voltage output of the generator is high enough, it can measure frequency as low as 1 Hz.

**III HARDWARE IMPLEMENTATION**

The circuitry for the frequency measurement is shown in Fig. 3. It is adapted to an Intel 8086 microprocessor-based system. With a slight change, it can also be adapted to other microprocessor-based systems. The numbers in circles in this figure relate to Fig. 4 which shows the sequential operation of the device.

The original signal is from the potential transformer (pt) connected to the terminals of the generator. This signal is first fed to an isolation transformer to isolate the digital side. Then the isolated signal goes through a filter and a voltage limiter. The filter removes the high frequency harmonics from the signal. The voltage limiter plays a very important role. The governor not only measures the frequency during the normal generation operation but also has to measure the frequency during the start-up and shut-down operations. During the start-up, the output voltage is produced by the residual magnetism from previous excitation and is very low. The ratio of the isolation transformer should be small. But after the start-up and the excitation of the generator, the output voltage of the generator goes up to the normal value and the output voltage of the pt is 220V (or 110V). So the voltage limiter is necessary in this case.

The limited signal (point 2 in Fig. 3) is shaped by a low offset voltage comparator. The output of the comparator (point 3 in Fig. 3) is a square wave. It can be adapted to TTL or CMOS circuitry. Then the frequency is divided by 2. The divider is composed of a D flip-flop. The true output of the D flip-flop (point 4 in Fig. 3) goes to the Gate pin of the timer (Intel 8253/8254). Its rising edge stops the timer and the falling edge stops the timer. During the timing, the timer counts the pulse of the Clk (point 1 in Fig. 3, a constant high frequency signal generated by a crystal).

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Another way is the method used in this paper (Fig. 3). The output signal of the timer (point 6 in Fig. 3) is connected to the interrupt controller. When the timer overflows, the microprocessor adds 1 to an extending counter in RAM and reloads the timer. In this way, the lowest frequency which can be measured by this circuitry mainly depends on the voltage output of the generator, e.g. if the voltage output of the generator is high enough, it can measure frequency as low as 1 Hz.

Generally, higher resolution can be obtained with higher clock frequency. But the Out interrupt should not happen around the supply frequency because:

1) In a real time controller, the interrupt is disabled during the execution of some important programs. So the interrupt can not be determined very accurately.
2) The interrupt is one of the entries of external disturbances to the microprocessor.
3) The time is a very critical resource in a real-time control system. Too frequent interrupts are not expected.

If no out interrupt happens over 45.00 Hz, the highest clock frequency is about 2.95 MHz. The \( f_c \) in the research prototype is 1193181 Hz (CPU clock/4).

The operation of the timer described above shows that the frequency measurement is executed once every two cycles. It can be easily modified to one measurement per cycle by using two timers. One
Before the generator synchronizing circuit breaker is closed, for fast synchronization with the electrical network the governor regulates the speed of the generating unit according to the network frequency (if the network frequency is normal) instead of the frequency set point. Therefore, the governor has to measure the network frequency as well. The circuitry is the same as that for the generator frequency except the Out interrupt. Normally, the network frequency is around 60 Hz (or 60 Hz). So, the Out interrupt is not necessary for the measurement of network frequency.

In the research prototype, there are independent measurement mechanisms for generator frequency and network frequency on each subsystem as shown in Fig. 5. From reliability consideration, there are four isolation transformers and each of them is connected to a different pt.

IV SOFTWARE IMPLEMENTATION IN DUPLICATE MICROPROCESSOR-BASED GOVERNOR

In the duplex microprocessor-based governor, each subsystem has its own frequency measurement hardware. In this section, the software for frequency calculation, error detection and fault tolerance is discussed.

1. Initialization of Timer and of Interrupt Controller:

The channels of the timer for frequency measurement are set in mode 0. The maximum counting value 0000H is loaded at the beginning and this value is reloaded at each falling edge of the Gate signal (the end of this sampling period) for the next sampling period.

While the frequency measured is below \( f_{i} \), the Out interrupt will occur. At each rising edge of the Out signal, the corresponding channel is reloaded with a value \( X \). This value is obtained from the following formula:

\[
X = 10000H - \text{Hex}(T_{i} \cdot f_{c})
\]  

Here, \( T_{i} \) is the time from the falling edge of the Out signal to its rising edge (Fig. 4). \( T_{i} \) is estimated according to the number of clock pulses that the microprocessor takes from the interrupt request to the end of the out command of the high byte of \( X \).

The interrupt controller is set in the edge interrupt mode. When the microprocessor is ready to measure a frequency, the corresponding interrupt masking bit in the interrupt controller is reset (unmasked).
2. Frequency Calculation:

Let \( N \) represent the count number of the timer. Then the frequency measured is:

\[
f = f_c / N.
\]  

The software diagram for frequency calculation is shown in Fig. 6. It is an interrupt subroutine. Because Intel 8253/8254 is down counting timer, the real count value \( (N) \) is the complement of the result \( (N_t) \) in the timer plus \( 10000H \) multiplied by the value \( (N_r) \) in the extending counter in RAM. For network frequency, \( N_r \) is always equal to zero.

\[
N = \text{NEG}(N_t) + 10000H * N_r
\]  

3. Error Detection:

A filter is generally used in the measurement. However it usually causes considerable delay and also complicates the implementation. In the duplex microprocessor-based governor, the error detection is used for the frequency measurement instead of filter. The rule of the error detection can be described as:

Because of the inertia of the turbine and the generator, the possible maximum change of the frequency in time delta \( T \) must be smaller than \( \delta \).

Supposing delta \( T \) is equal to 1 s and \( f(k-1) \) is the frequency of the last sampling cycle, the lower limit of the frequency \( f(k) \) in this sampling cycle is:

\[
f_l = f(k-1) - 2 \delta / f(k-1)
\]  

and the upper limit is:

\[
f_u = f(k-1) + 2 \delta / f(k-1)
\]  

Here \( 2 \delta / f(k-1) \) is the time interval between these two consecutive sampling periods. If the frequency measured is wrong in \( m \) consecutive sampling periods, the lower limit of the frequency \( f(k+m) \) can be obtained from the following recurrence formula:

\[
f_{li}(i) = f_{li}(i-1) - 2 \delta / f_{li}(i-1)
\]  

and the recurrence formula for the upper limit is:

\[
f_{ui}(i) = f_{ui}(i-1) + 2 \delta / f_{ui}(i-1)
\]  

\( i = 1, 2, ..., m \). Actually after \( m \) has reached a certain value, for example 3, the frequency measurement is considered faulty.

Due to the short sampling period, this error detection method is very effective. \( \delta \) can be pre-determined according to the inertia of the generating unit and the maximum operating speed of the guide blade. \( \delta \) for the network frequency is generally smaller than that for the generating unit frequency. \( \delta \) should initially be large. It can be modified on line according to preset rules.

4. Fault Tolerance:

The frequency information flow in the duplex microprocessor-based governor is shown in Fig. 7. Each module samples the frequency independently and passes the result (the count value) to the other module. It also gets the sampling result from the other module. So there are two values for the same frequency in each module at each sampling period. The following steps are adopted to implement the fault tolerance of frequency measurement in each module.

Step 1: The frequency input by this module \( (f_1) \) is detected. If it is normal, clear its error counting and its faulty flag. Otherwise, add 1 to the error counter. If the error counting number is larger then \( N \), a fault flag for \( f_1 \) is set.

Step 2: The frequency input by the other module \( (f_2) \) is detected. If it is normal, clear its error counting and its faulty flag. Otherwise, add 1 to the error counter. If the error counting number is larger then \( N \), a fault flag for \( f_2 \) is set.

Step 3: When the error counters for \( f_1 \) and \( f_2 \) are zero, the frequency of this sampling period in this module is: \( f = (f_1 + f_2) / 2 \). Go to step 6.

Step 4: When the error counter for \( f_1 \) is zero and that for \( f_2 \) is a non-zero positive integer, then \( f = f_2 \) and vice versa. If the error counters for both \( f_1 \) and \( f_2 \) are non-zero positive integer, there is no updated \( f \) in this sampling period.

Step 5: Display the fault information when any faulty flag has been set. If both fault flags have been set, go to step 7.

Step 6: Wait for frequency input interrupt. When this module receives the frequency input interrupt, go to step 1. If there is no frequency input interrupt in time \( T_7 \), the two fault flags will be set and the next step will be executed.

Step 7: The alarm is sounded and proper strategy...
is adopted [14].

Note 1. Each module separately detects frequency by use of the means proposed in 3 (Error Detection). The frequency input by subsystem 1 (i=1) or 2, 1 represents this subsystem and 2 represents the other subsystem) is detected by both subsystems. The rules proposed in Ref. [14] are used for the resolution of any dispute between the two subsystems.

1. If there is no frequency information from subsystem i in a sampling period, it is treated as wrong information.

2. Tz=r*N. where r is sampling period.

3. Test'N, where t is sampling period.

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Figure 7 Frequency Information Flow in Duplex Microprocessor-Based Governor

V PERFORMANCE AND TEST RESULTS

Test results of the frequency measurement performance and the fault tolerance of the frequency measurement in the research prototype are presented below.

1. Resolution.

For a clock frequency of 1193181 Hz, the resolution is about 0.004 percent at 50.00 Hz. Test results are shown in Tab. 1.

Table 1 Resolution Test Results (samples in 9 consecutive periods).

<table>
<thead>
<tr>
<th>No.</th>
<th>COUNT NUMBER</th>
<th>FREQUENCY ON DISPLAY</th>
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<td>23863</td>
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If an 8-bit extending counter is set in RAM, the low limit of the measuring range is about 0.1 Hz. Its high limit is about 119 Hz with 0.01 percent resolution. However, in this special application the low limit depends on the voltage of the input signal (as discussed in section 3).

Test 1. Low voltage signal input test.

Test step and result: Using a sine signal generator, the output frequency was set at 10 Hz and the output voltage of the signal generator was adjusted. For the output of the isolation transformer larger than 0.12 V, the measurement was stable. When this voltage was under 0.08 V, the measurement failed.

Test 2. High voltage signal input test.

Test step and result: Connecting the isolation transformer to a.c. power source via an adjustable transformer, the voltage of the isolation transformer was raised up to 220 V. The measurement circuitry worked normally.

3. The Speed of Response.

The speed of response of the measurement is dependent upon the frequency measured. It is equal to 2/f.

4. Fault Tolerance Test.

Test 1. The failure of the frequency measurement of the on-line subsystem.

Initial state: the frequency measurements of both subsystems were operating normally. Subsystem A was the on-line subsystem and subsystem B was standby.

Test steps and phenomena: 1) The frequency signal to subsystem A was cut off but it remained the on-line subsystem. Display indicated the frequency measurement of subsystem A as faulty. 2) The frequency was then changed. The control output of the system, i.e. the output of subsystem A, responded correctly.

Test 2. The failure of the frequency measurement on the standby subsystem.

Initial state: same as Test 1.

Test steps and phenomena: 1) The frequency signal to subsystem B was cut off. Subsystem A remained the on-line subsystem. Display indicated the frequency measurement of subsystem B as faulty. 2) The frequency was then changed. The control output of subsystem B responded correctly.

Test 3. The generator frequency measurement on the on-line subsystem failed and the network frequency measurement on the standby subsystem failed (or vice versa).

Initial state: same as Test 1.

Test steps and phenomena: 1) The generator frequency signal to subsystem A and the network frequency signal to subsystem B were cut off. Subsystem A remained the on-line subsystem. Display indicated the generator frequency measurement of subsystem A and the network frequency measurement of subsystem B as faulty. 2) Both generator frequency and network frequency were changed. The control outputs of two subsystems responded correctly.

Test 4. The generator frequency measurement of both subsystems failed.

Initial state: same as Test 1.

Test steps and phenomena: The generator's frequency to both subsystems was cut off. The alarm was sounded and the governor moved to manual operation state.

Test 5. Frequency measurement recovery from fault.

Test step and phenomenon: With the system in one of the 4 faulty states simulated in Tests 1'4, the signal(s) was reconnected. The system went back to the initial state.
5. Error Detection.

Test step and phenomena: With the governor operating in stable state, intermittent electromagnetic disturbances were induced around the measurement circuitry. The output of frequency divider and the control output of the system were observed. When the output of the frequency divider was obviously disturbed, the control output still remained stable.

The above test results show that the frequency measurement in the research prototype of the duplex fault-tolerant governor has met the design specifications.

VI CONCLUSIONS

The frequency measurement technique proposed in this paper has wide measuring range, fast response and high resolution. It is specially designed for digital governors. It can also be used in other applications where the frequency measurement of the electric power is needed. One such application example, an Intelligent Frequency Measurement Meter for Electric Power Industry developed by a Chinese electronics manufacturer is based on this frequency measurement technique. This meter is implemented in an Intel single chip microprocessor.

REFERENCES


4. ACEC DESCRIPTION "A NEW GENERATION SPEED GOVERNOR: ACEC-MemoRHY FOR WATER TURBINE" NDA 557-00-30;


12. YE Luqing, WEI Shouping, LI Zhaohui, O.P.Malik & G.S.Hope "Field Test and Operation of a Duplicate Multiprocessor-based Governor for Water Turbine and Its Further Development" Accepted for presentation at IEEE PES 1990 Winter Meeting.


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