Making Sense of Atmel XMega Series

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This tutorial addresses features, not programming or electrical details. A brief discussion of some hardware differences compared to Mega devices is at the end.

Generic XMega - The Atmel XMega line of microcontrollers might be thought of as a "super-set" of the Mega line. Allowed clock speeds are higher, there are more peripherals, like UARTs and timers, and there are some fairly unique features. ALL have a maximum operating voltage of 3.6V. With one exception, minimum operating voltage is 1.6V.

All have the standard AVR 8-bit data & 16-bit RISC instruction set that is a superset of the standard Mega/Tiny controller instruction set.

What They All Have: There are some features that all share.

- Watchdog timer
- Brown-out Detector
- Calibrated RC oscillator (good enough for clocking a UART)
- Real-Time clock (counter and provisions for external crystal)
- Multiple PWM channels (at least 8)
- Multiple input capture channels (at least 8)
- Multiple output compare channels (at least 8)
- Multiple timers (at least 2)
- Debugging (at least PDI)
- PicoPower
- Self programming capability with a separate, protected, bootload memory section that is not counted in the regular flash memory size
- Temperature sensor
- Analog comparators (at least 2)
- ADC - 12 bit, fast (relative to Mega/Tiny) at least 200Ksamples/sec and at least 8 multiplexed inputs
- TWI (I2C) (at least 1), usually with address detection
- SPI (at least 1)
- Multiple external interrupts (at least 26)
- Event system
- Faster CPU clock (relative to Mega/Timy) 32MHz, maximum @Vcc=3.6V
- DMA

What They All Do Not Have: These are from Atmel's on-line selector guide so Atmel chose to list them as features that none of the devices have (at the time of this writing).

- No MMU/MPU
- No FPU
- No NAND interface
- No Resistive touch controller
- No Camera interface
- No Video decoder
- No graphic LCD interface
- No ethernet interface
- No I2S interface
- No LIN interface
- No CAN interface
- No Hardware Q-Touch interface

Packages: There are standard pin-count and package combinations. These are shown in the next table. Hobby users will be disappointed that there is not a single DIP-packaged device in the lot. From that standpoint, this is a "pro" line though hobbyists are learning how to use the TQFP packages.

Pin Count	TQFP	QFN	BGA
100	TQFP-100 (14mmX14mm)		BGA-100 (9mmX9mm & 7mmX7mm)
64	TQFP-64 (14mmX14mm)	QFN-64 (8mmX9mm)	
44	TQFP-44 (10mmX10mm)	QFN-44 (7mmX7mm)	BGA-49 (5mmX5mm)
32	TQFP-32 (7mmX7mm)	UQFN-32 (4mmX4mm) VQFN-32 (5mmX5mm)	

Memory Size - Atmel now consistently numbers its devices by memory size. For example, an XMega64A1 is essentially the same as an XMega128A1, the latter having 128K of flash memory while the first has 64K of flash. Thus, if you are using a 32C3, and need more memory space, the next larger would be 64C3 and almost everything else inside remains the same.

Atmel is also quite consistent in combinations of memory sizes. Here are the combinations you will find. The "Boot" memory is a separate amount of bootloader flash on top of the program flash listed in the first column.

Flash	Boot	SRAM	EEPROM
384K	8K	32K	4096
256K	8K	16K	4096
192K	8K	16K	2048
128K	8K	8K	2048
64K	4K	4K	2048
32K	4K	4K	2048 / 1024
16K	2K	4K/3.3K/2K	1024 / 512
8K	2K	1K	512

Families - There are 5 “series” within the XMega family, A, B, C, D, and E. There is a broad set of common features across all A devices that is different than B devices, and so-forth. In some cases, there are sub-series. An example is A1, A3, and A4. And, for all practical purposes, there can a sub-sub-series (A1 and A1U, for example). There are feature distinctions between, say, A1 and A3 and more than just USB on A1U compared to A1.

Here is a listing of the common features (in addition to the generic XMega features) for each series:

- A-series (“high performance” series) All include
  - Dual (independent) ADC
  - DAC, 12 bit
  - AES/DES crypto engine
  - Multiple UARTs, SPIs, I2Cs

- B-Series (“LCD controller” series) All include
  - LCD segment controller, 4x25 or 4x40
  - Full-speed USB
  - Dual (independent) ADCs

- C-Series (”Entry level USB” series) All include
  - Full-speed USB

- D-Series (“Entry level/low power” series) All include
  - 12-bit ADC, multiple channels, 200KSamples/sec

- E-Series (“Small package” series) All include
    - DAC, 2 channels, 1 MSample/sec
    - ADC, 16 channels, 300KSamples/sec
    - TWI fast mode (1MHz)
    - Custom Logic (XCL)
    - System wakeup from UART

Documentation - this is a sore point among many Mega/Tiny users who attempt to migrate to XMega devices. Mega/Tiny devices have a single, unified, spec sheet for each device or group of devices. With XMega, it is split with a “Series Manual” for A, B, C, D, and E series, and specific manual for each sub-series. YOU NEED BOTH! The xxxA1 manual does not tell you everything that the A-Series manual does, and visa-versa! And the xxxA1U manual has details about USB (and other things) that the xxxA1 manual does not.

By Sub-series - in the following, “xAy” should be read as “x” indicating a variety of flash sizes, “A” indicates the series, “y” indicates the sub-series (as in “1” or “1U”). For each sub-series listed, the available flash sizes are shown as “(256/128/64)”. The various memory types are not listed since the previous table shows all of the combinations, keyed by flash size. Note that this should NOT be taken as a definitive list; consult the specification manuals for for the official feature list.

- **xA1 -** (128/64) **Not recommended for new designs.**
    - 8x 16 bit timer/counter
    - 8x USART (one with IRDA interface)
    - High resolution (PLL clock mult) for 2 timers
    - Advanced Waveform Extension for 2 timers
    - 4x TWI(I2()/SMBus interfaces
    - 4x SPI interfaces
    - AES & DES Crypto Engine
    - 16 bit Real-Time Clock
    - 2x 16 channel, 12-bit, 2MS/sec ADC
    - 2x 2 channel, 12-bit, 1MS/sec DAC
    - 4x Analog Comparator
    - external sdram interface
    - JTAG and PDI debugging

- **xA1U -** (128/64) Like the xA1 with the following notable differences:
    - Recommended for new designs
    - 1 Full-speed USB 2.0 DEVICE interface (not master)
    - CRC-16 and CRC-32 generator
    - 3x quadrature decoder channels

- **xA3 -** (256/192/128/64) **Not recommended for new designs.**
    - 7x 16 bit timer/counter

- 7x USART (one with IRDA interface)
- High resolution (PLL clock mult) for all timers
- Advanced Waveform Extension for 1 timers
- 4x TWI(I2()/SMBus interfaces with address detectors
- 3x SPI interfaces
- AES & DES Crypto Engine
- 16 bit Real-Time Clock
- 2x 8 channel, 12-bit, 2MS/sec ADC
- 1x 1 channel, 12-bit, 1MS/sec DAC
- 4x Analog Comparator
- JTAG and PDI debugging

- **xA3U -** (256/192/128/64) Like the xA3 with the following notable differences:
  - Recommended for new designs
  - 1 Full-speed USB 2.0 DEVICE interface (not master)
  - CRC-16 and CRC-32 generator
  - 3x quadrature decoder channels

- **xA3B -** (256) **Not recommended for new designs.**
  - 7x 16 bit timer/counter
  - 6x USART (one with IRDA interface)
  - High resolution (PLL clock mult) for all timers
  - Advanced Waveform Extension for 1 timers
  - 2x TWI(I2()/SMBus interfaces with address detectors
  - 2x SPI interfaces
  - AES & DES Crypto Engine
  - 16 bit Real-Time Clock
  - 2x 8 channel, 12-bit, 2MS/sec ADC
  - 1x 1 channel, 12-bit, 1MS/sec DAC
  - 4x Analog Comparator
  - JTAG and PDI debugging

- **xA3BU -** (256) Like the xA3B with the following notable differences:
  - Recommended for new designs
  - 1 Full-speed USB 2.0 DEVICE interface (not master)
  - CRC-16 and CRC-32 generator
  - 3x quadrature decoder channels

- **xA4 -** (128/64/32/16) **Not recommended for new designs.**
  - 5x 16 bit timer/counter
  - 5x USART (one with IRDA interface)
  - High resolution (PLL clock mult) for all timers
  - Advanced Waveform Extension for 1 timers
  - 2x TWI(I2()/SMBus interfaces with address detectors
  - 2x SPI interfaces
  - AES & DES Crypto Engine

- 16 bit Real-Time Clock
- 1x 12 channel, 12-bit, 2MS/sec ADC
- 1x 2 channel, 12-bit, 1MS/sec DAC
- 2x Analog Comparator
- PDI debugging

- **xA4U-** (128/64/32/16) Like the xA4 with the following notable differences:
  - Recommended for new designs
  - 1 Full-speed USB 2.0 DEVICE interface (not master)
  - CRC-16 and CRC-32 generator
  - 3x quadrature decoder channels

- **xB1 -** (128/64)
  - 3x 16 bit timer/counter
  - 2x USART (one with IRDA interface)
  - High resolution (PLL clock mult) for 1 timer
  - Advanced Waveform Extension for 1 timer
  - Split mode for 2 timers
  - 1X USB 2.0 device (not master)
  - 2x TWI(I2()/SMBus interfaces with address detectors
  - 2x SPI interfaces
  - AES & DES Crypto Engine
  - CRC-16 & CRC-32 generator
  - LCD driver up to 4x40
  - 16 bit Real-Time Clock
  - 2x 8 channel, 12-bit, 300KS/sec ADC
  - 4x Analog Comparator
  - JTAG & PDI debugging

- **xB3 -** (128/64)
  - 2x 16 bit timer/counter
  - 1x USART (one with IRDA interface)
  - High resolution (PLL clock mult) for 1 timer
  - Advanced Waveform Extension for 1 timer
  - Split mode for 2 timers
  - 1X USB 2.0 device (not master)
  - 1x TWI(I2()/SMBus interfaces with address detectors
  - 1x SPI interfaces
  - AES & DES Crypto Engine
  - CRC-16 & CRC-32 generator
  - LCD driver up to 4x425
  - 16 bit Real-Time Clock
  - 2x 8 channel, 12-bit, 300KS/sec ADC
  - 2x Analog Comparator
  - JTAG & PDI debugging

- **xC3 -** (256/192/128/64/32)
  - 5x 16 bit timer/counter
  - 3x USART (one with IRDA interface)
  - High resolution (PLL clock mult) for 2 timer
  - Advanced Waveform Extension for 1 timer
  - 1X USB 2.0 device (not master)
  - 2x TWI(I2()/SMBus interfaces with address detectors
  - 2x SPI interfaces
  - CRC-16 & CRC-32 generator
  - LCD driver up to 4x425
  - 16 bit Real-Time Clock
  - 1 16 channel, 12-bit, 300KS/sec ADC
  - 2x Analog Comparator
  - PDI debugging

- **xC4 -** (32/16)
  - 4x 16 bit timer/counter
  - 3x USART (one with IRDA interface)
  - High resolution (PLL clock mult) for 2 timer
  - Advanced Waveform Extension for 1 timer
  - 1X USB 2.0 device (not master)
  - 2x TWI(I2()/SMBus interfaces with address detectors
  - 2x SPI interfaces
  - CRC-16 & CRC-32 generator
  - LCD driver up to 4x425
  - 16 bit Real-Time Clock
  - 1 16 channel, 12-bit, 300KS/sec ADC
  - 2x Analog Comparator
  - PDI debugging

- **xD3 -** (384/256/192/128/64/32)
  - 5x 16 bit timer/counter
  - 3x USART (one with IRDA interface)
  - High resolution (PLL clock mult) for 2 timer
  - Advanced Waveform Extension for 1 timer
  - 2x TWI(I2()/SMBus interfaces with address detectors
  - 2x SPI interfaces
  - CRC-16 & CRC-32 generator
  - 16 bit Real-Time Clock
  - 1 16 channel, 12-bit, 300KS/sec ADC
  - 2x Analog Comparator
  - PDI debugging

- **xD3_Auto -** (64)
  - Like xD3 but specified for extended environmental range

- **xD4 -** (128/64/32/16)
  - 4x 16 bit timer/counter
  - 2x USART (one with IRDA interface)
  - High resolution (PLL clock mult) for all timer
  - Advanced Waveform Extension for 1 timer
  - 2x TWI(I2()/SMBus interfaces with address detectors
  - 2x SPI interfaces
  - CRC-16 & CRC-32 generator
  - 16 bit Real-Time Clock
  - 1 12 channel, 12-bit, 200KS/sec ADC
  - 2x Analog Comparator
  - PDI debugging

- **xE5 -** (32/16/8)
  - 3x 16 bit timer/counter
  - 2x USART (one with IRDA interface)
  - High resolution (PLL clock mult) for all timer
  - Advanced Waveform Extension for 1 timer
  - Timer fault extension for control of external drivers
  - 2x TWI(I2()/SMBus interfaces with address detectors
  - 1x SPI interfaces
  - CRC-16 & CRC-32 generator
  - 16 bit Real-Time Clock
  - 1 16 channel, 12-bit, 300KS/sec ADC
  - 1 2 channel 12-bit 1MS/sec ADC
  - 2x Analog Comparator
  - XCK custom logic module
  - PDI debugging

The XMega Register System - A big struggle for Mega/Tiny programmers is the register system in the XMega. Or, more specifically, the struggle is about how to access those registers.

Some facts may help to simplify this a little. Unlike Mega/Tiny devices, the registers for each “peripheral” (timer, USART, and such) are located in a block. The blocks for all timers are arranged identically. Same for USARTs, Same for TWI, SPI, and so on. Thus, any functional register can be referred to by the address of the start of the block plus some offset. The offset pattern is the same for all timers, for all USARTs and so forth. Further, the bit locations are identical in all the registers of a given function. So, to access a given bit, we need to know the name of the peripheral device (determines the base address), the register name (determines the offset) and the bit name.

Now, we have a bit of a problem. How this is handled is different for assembler and for C/C++. Consider the “CTRL” register inside the “CLK” (peripheral) module. For assembler, there are names such as CLK_CTRL. In C/C++, they are accessed as a struct and that register would be CLK.CTRL

You can find much more in Atmel's Application Note "AVR1000: Getting Started Writing C-code for the XMEGA".

The XMega Clock System - Another of the things that will confuse Mega/Tiny users is the XMega clock system. This system is quite consistent across the entire XMega line.

As with all of the Mega/Tiny devices, there is a significant range of choices for clock source. BUT, we need to be careful, here. There can be multiple clock frequencies running around, inside an XMega. Not all of the possible clock sources can be used for every purpose. The possible clock sources are:

- External crystal oscillator, 0.4MHz to 16MHz
- External 32.768KHz crystal oscillator
- An external clock (signal) source
- Internal 32KHz Ultra Low Power (non-crystal) oscillator with 1KHz output
- Internal 32.768 Calibrated (non-crystal) oscillator
- 2MHz "Run-Time Calibrated" oscillator
- 32MHz "Run-Time Calibrated" oscillator
- A phase-locked loop (PLL) multiplier to generate a system clock at 1X to 31X the source frequency
- A phase-locked loop (PLL) multiplier to generate a clock at 2X or 4X the CPU clock frequency

After a reset, the CPU ALWAYS starts using the 2MHz internal oscillator. User-written software determines which clock will be used after start-up and when the switch occurs.

The internal 32KHz Ultra Low Power oscillator is always on when there is power, even during reset. It is divided by 32 to make a 1KHz signal that is always used for the watchdog and for the brown-out detector. It can optionally be used for the RealTime Clock.

The internal 32.768KHz non-crystal oscillator is divided by 32 and can be used for the RealTime Clock. Undivided, it can be the "system clock".

The external 32.768 Crystal Oscillator is divided by 32 and can be used divided or undivided, for the RealTime Clock.

The external clock signal and the external 0.4MHz to 16MHz crystal oscillator are mutually exclusive. You can use one or the other but not both. Three signals, 32.768KHz external, clock external, or 0.4-16MHz external are multiplexed and useable EITHER as system clock or as an input to the frequency multiplier PLL.

The internal 32MHz oscillator can be used as system clock or, divided by 4, as an input to the frequency multiplier PLL.

The internal 2MHz oscillator can be used as a system clock or as an input to the frequency multiplier PLL.

AND, the output of the frequency multiplier PLL, multiplying its input frequency by an integer value from 1 to 31, can provide the system clock.

The system clock can then be divided, through a number of independent System Clock Prescalers, for a variety of uses, from CPU to SRAM and peripherals.

What is missing from this list is the fast 2X/4X PLL multiplier for the “high-resolution extension” for faster PWM generation by counters. This is part of the counter block and not the clock distribution.

All of these clock components should be fairly obvious except “Why that multiplier PLL? What good is it?” Well, you could use it to generate a system clock of 1.015MHz from an external watch crystal oscillator (32768Hz x 31). You could also use it to generate faster clocks above 2MHz up to 32MHz. Even though it might seem possible to generate 2MHz X 31 = 62MHz, that would violate the 32MHz clock limit.

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Finally, lets mention the “Run-Time Calibrated” 2MHz and 32MHz internal oscillators. They are not “calibrated” in the usual sense, but are each controlled by a “digital frequency loop” that compares their frequency to the internal calibrated 32.768KHz oscillator or an external oscillator (usually 32.768KHz). This process is not as precise as a phase-locked loop but it uses much less power. The end result is that using either the internal 2MHz or internal 32MHz oscillators is sufficiently accurate to provide the clock for a UART.

The XMega General Purpose IO Structure - This is another point that Mega/Tiny users may stumble over. The Mega/Tiny devices allow input, with or without pullup, output high, output low. That is it. Further, specialized inputs or outputs (such as PWM or input capture) are fixed to specific pins.

The XMega provides pin mapping for many I/O functions. That is one big difference. But, the general purpose I/O (GPIO) capability is also much more extensive. It includes:

- Floating input
- Input with pull-up
- Input with pull-down
- Totem pole output (normal CMOS logic output)
- Wired OR (with optional pull-down) - open drain PChannel pull-up
- Wired AND (with optional pull-up) - open drain NChannel pull-down.

- Bus Keeper output - a “soft latch” that holds the output in its previous state, even if the output driver should be turned off.
- Output slew-rate control

As one might expect, there are more registers to deal with on all these options. Each port is in a separate block, as described in the previous section. The port control and access registers are the same for every port. These registers are accessed with block names of PORTA, PORTB, and so forth.

On the input side, every pin can be sensed for level and for change, in a variety of ways.

Check the Errata: Near the end of every device-specific manual, there is a list of errata. Check it. The lists, especially on early parts, can be quite extensive.No matter what you are working on, there are good odds that there will be something in that list that effects you!