AVR Freaks

DESIGN NOTE #022

AUTHOR: AVRFREAKS

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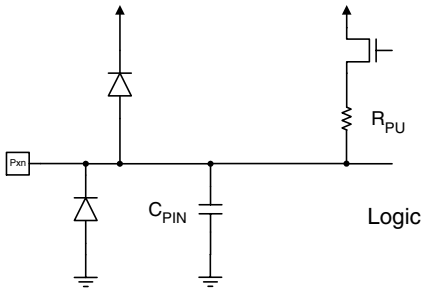
I/O Port Details

Introduction

This document may help to shed some light on how the AVR® input stages works. Hardware engineers may find it especially useful when designing and debugging their systems.

Overview

Figure 1. I/O Pin Equivialent schematic



Pad

The pad offers a small input capacitance. Usually ignored, but should be considered when calculating rise and fall times of large data busses. Min and max capacitor values are stated in the respective datasheet.

Input Protection

Along with the usual protection diodes to GND and V_{CC}, the input protection also features a series resistor. The resistor is included to protect the pad from electrostatic discharge (ESD) currents. ESD pulses could otherwise result in overheating and permanent damage. For all practical calculations, the series resistor may be ignored. No characterization data is available for this resistor.

Analog Control

The optional pull-up resistor can be connected by correct configuration of PORTx and DDRx bits. It will offer a large pull-up resistor to V_{CC} to keep the line stable high when no external source is connected. Enabling the pull-up resistor for open inputs (no external source connected) is always recommended, as it prevents the pin from oscillating when picking up surrounding noise.

For analog inputs (Analog Comparator, Analog-to-Digital Converter), the signal will be fed into the analog modules with no further conditioning.

Digital Delay

Although not many are aware of it, all AVR digital Inputs have a delay of 1.5 clock cycles through the synchronizing logic. This logic is necessary to prevent undefined logic levels feeding into the digital logic inside the devices.