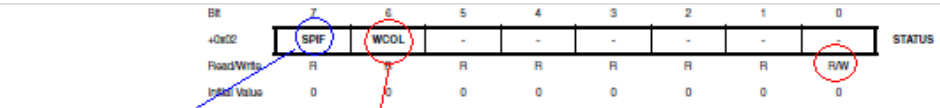

Bit	7	6	5	4	3	2	1	0	
+0x02	SPIF	WCOL	-	-	-	-	-	-	STATUS
Read/Write	R	R	R	R	R	R	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 - IF: SPI Interrupt Flag**

When a serial transfer is complete and one byte is completely shifted in/out of the DATA register, the IF bit is set. If SS is an input and is driven low when the SPI is in Master mode, this will also set the IF bit. The IF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, the SPIF bit can be cleared by first reading the STATUS register with IF set, and then access the DATA register.

SPIF

WRCOL

XMEGA A

- **Bit 6 - WRCOL: Write Collision Flag**

The WRCOL bit is set if the DATA register is written during a data transfer. The WRCOL bit is cleared by first reading the STATUS register with WRCOL set, and then accessing the DATA register.

- **Bit 5:0 - Reserved**

These bits are reserved and will always be read as zero. For compatibility with future devices, always write these bits to zero when this register is written.

20.7.4 DATA - SPI Data Register

Bit	7	6	5	4	3	2	1	0	
+0x03	DATA[7:0]								DATA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The DATA register used for sending and receiving data. Writing to the register initiates the data transmission, and the byte written to the register will be shifted out on the SPI output line. Reading the register causes the Shift Register Receive buffer to be read, and return the last bytes successfully received.

20.8 Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
+0x00	CTRL	CLK2X	ENABLE	DORD	MASTER	MODE[1:0]		PRESCALER[1:0]		232
+0x01	INTCTRL	-	-	-	-	-	-	INTLVL[1:0]		233
+0x02	STATUS	IF	WRCOL	-	-	-	-	-	-	233