26.8 Low Power mode

To reduce the power consumption in DAC conversions, the DAC may be set in a Low Power mode. In Low Power mode, the DAC is turned off between each conversion. Conversion time will be longer if new conversions are started in this mode. To put the DAC into low power mode, you need to set the bit 1 in CTRLA register (called DACCRA).

26.9 Calibration

To achieve optimal accuracy, it is possible to calibrate both gain and offset error in the DAC. There is a 7-bit calibration value for gain adjustment and a 7-bit calibration value for offset adjustment.

To get the best calibration result it is recommended to use the same VREF, output channel selection, sampling time, and refresh interval when calibrating as will be used in normal DAC operation. The theoretical transfer function for the DAC was shown in "Overview" on page 317. Including errors, the DAC output value can be expressed as:

$$V_{DACxX} = gain \cdot \frac{CHnDATA}{0xFFF} + offset \qquad V_{DACxX} = gain \cdot \frac{CHnDATA}{0xFFF} \cdot VREF$$

In an ideal DAC, gain is 1 and offset is 0.

The calibration of the DAC adjust the offset and gain. To calibrate offset you can output mid code and adjust the offset calibration until you get ~0 LSB offset The gain is adjusted around mid code so it should not affect the offset calibration if you read the output at mid code and max (or min code) and adjust the calibration values until you get ~0 LSB gain.

26.10 Register Description

26.10.1 CTRLA – DAC Control Register A

Bit	7	6	5	4	3	2	1	0	
+0x00	-	-	-	IDOEN	CH1EN	CH0EN	-	ENABLE	CTRLA
Read/Write	R	R	R	R/W	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit	7	6	5	4	3	2	1	0	
+0x00	-	-	-	IDOEN	CH1EN	CH0EN	-	ENABLE	CTRLA
Read/Write	R	R	R	R/W	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7:5 - Reserved**

These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.

- **Bit 4 - IDOEN: DAC Internal Output Enable**

Setting this bit routs the internal DAC output to the ADC and Analog Comparator MUXes.

- **Bit 3 - CH1EN: DAC Channel 1 Output Enable**

Setting this bit will make channel 1 available on pin while clearing the bit makes channel 1 only available for internal use.

- **Bit 2 - CH0EN: DAC Channel 0 Output Enable**

Setting this bit will make channel 0 available on pin while clearing the bit makes channel 0 only available for internal use.

- **Bit 1 - Res - Reserved**

This bit is unused and reserved for future use. For compatibility with future devices, always write this bit to zero when this register is written.

- **Bit 0 - ENABLE: DAC Enable**

This bit enables the entire DAC.

26.10.2 CTRLB – DAC Control Register B

Bit	7	6	5	4	3	2	1	0	
+0x01	-	CHSEL[1:0]		-	-	-	CH1TRIG	CH0TRIG	CTRLB
Read/Write	R	R/W	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 - Reserved**

This bit is unused and reserved for future use. For compatibility with future devices, always write this bit to zero when this register is written.

- **Bits 6:5 - CHSEL[1:0]: DAC Channel Selection**

These bits control wether the DAC should operate with single or dual channel outputs. Table 26-1 shows the available selections.

Table 26-1. DAC channel selection

CHSEL[1:0]	Description
00	Single channel operation (for channel 0 only)
01	Reserved
10	Duel channel operation (S/H for channel 0 and channel 1)
11	Reserved

Dual

- **Bits 4:2 - Reserved**

These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.

- **Bit 1 - CH1TRIG: DAC Auto trigged mode Channel 1**

If this bit is set, the incoming event on the event channel selected in the EVCTRL Register will start the conversion when a new value is written to high byte of the data register CH1DATA.

Does not seem to be corrct.

- **Bit 0 - CH0TRIG: DAC Auto trigged mode Channel 0**

If this bit is set, the incoming event on the event channel selected in the EVCTRL Register will start the conversion when a new value is written to high byte of the data register CH0DATA.

26.10.3 CTRLC – DAC Control Register C

Bit	7	6	5	4	3	2	1	0	
+0x02	-	-	-	REFSEL[1:0]		-	-	LEFTADJ	CTRLC
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 3:0 - REFRESH[3:0]: DAC Channel Refresh Timing Control**

These bits control time interval between each time a channel is refreshed in dual channel (S/H) mode. The interval must be set relative to the Peripheral clock to avoid loosing accuracy of the converted value.

2.2.3 Sample Interval

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When using dual channel operation, there is a certain minimum time delay required from conversion of channel 0 starts until channel 1 can start. This is due to a finite settling time of the DAC conversion block output. This delay is minimum 1 µs, which limits the sample rate to maximum 1 MHz.

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16. **DAC has up to ±10 LSB noise in Sampled Mode**

The DAC has noise of up to ±10 LSB in Sampled Mode for entire operation range.

Problem fix/Workaround

Use the DAC in continuous mode.

17. **DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V**

Using the DAC with a reference voltage above 2.4V or VCC - 0.6V will give inaccurate output when converting codes that give below 0.75V output:

– ±10 LSB for continuous mode

– ±200 LSB for Sample and Hold mode

Problem fix/Workaround

None.

DAC Refresh may be blocked in S/H mode

18. **DAC has up to ±10 LSB noise in Sampled Mode**

If the DAC is running in Sample and Hold (S/H) mode and conversion for one channel is done at maximum rate (i.e. the DAC is always busy doing conversion for this channel), this will block refresh signals to the second channel.