- **Bit [3:2] - ERRINTLVL[1:0]: DMA Channel Error Interrupt Level**

These bits enable the interrupt for DMA channel transfer error select the interrupt level as described in Section 12. "Interrupts and Programmable Multi-level Interrupt Controller" on page 123. The enabled interrupt will trigger for the conditions when the ERRIF is set.

- **Bit [1:0] - TRNINTLVL[1:0]: DMA Channel Transaction Complete Interrupt Level**

These bits enable the interrupt for DMA channel transaction complete and select the interrupt level as described in Section 12. "Interrupts and Programmable Multi-level Interrupt Controller" on page 123. The enabled interrupt will trigger for the conditions when the TRNIF is set.

5.14.3 ADDRCTRL - DMA Channel Address Control Register

Bit	7	6	5	4	3	2	1	0	
+0x02	SRCRELOAD[1:0]		SRCDIR[1:0]		DESTRELOAD[1:0]		DESTDIR[1:0]		ADDRCTRL
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

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- **Bit 7:0 - TRFCNT[15:8]: DMA Channel n Block Transfer Count Register High byte**

These bits hold the 8 MSB of the 16-bits block transfer count.

The default value of this register is 0x1. If a user write 0x0 to this register and fire a DMA trigger, DMA will be doing 0xFFFF transfers.

5.14.6 TRFCNTL - DMA Channel Block Transfer Count Register L

Bit	7	6	5	4	3	2	1	0	
+0x04	TRFCNT[7:0]								TRFCNTL
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	1	1	1	1	1	1	1	1	

- **Bit 7:0 - TRFCNT[7:0]: DMA Channel n Block Transfer Count Register Low byte**

These bits hold the 8 LSB of the 16-bits block transfer count.

The default value of this register is 0x1. If a user write 0x0 to this register and fire a DMA trigger, DMA will be doing 0xFFFF transfers.