4¾ Digit Multi-Meter / Counter

FEATURES

- 4¾ digit display (± 29,999 max reading)
- 6 range autoranging
- Autozero, auto polarity
- Direct LED 7 segment drive
- Leading zero blanking/overrange blinking
- Multiplexed BCD output
- Single power supply
- On chip clock
- 20,000, 29,999 or freerun counter modes

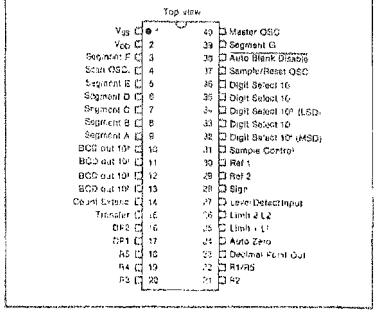
DESCRIPTION

The AY-3-3550 contains all the logic for a 4¾ digit DMM (±29,999 maximum reading) incorporating dual ramp integration. Outstanding features of this "state-of-the-art" DMM chip include 6 range autoranging, autozero, auto polarity, direct 7-segment LED drive, and multiplexed BCD outputs. An on-chip oscillator controls the sampling rate, digit select multiplexing and BCD counting.

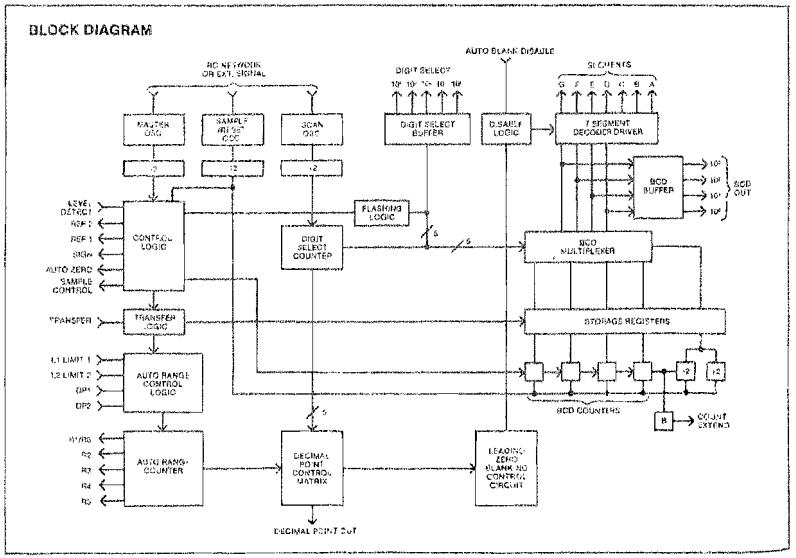
Fabricated in GI's advanced N-channel Ion Implant process to enable operation from a single power supply (+4.5V to +11V), the AY-3-3550 typically draws only 12mA when operating at +5V.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



Functional Description

Operation

(Refer to Figs. 1 and 2 and the Block Diagram) An input on the Sample/Reset OSC Input triggers the internal reset signal which in turn resets the internal BCD synchronous counters, synchronizes the master clock with the control signals and simultaneously activates the 10¹ Multiplex output. At the first master clock following the trailing edge of the internal reset, the 'Sample Control' signal is activated. This signal opens the switch in the analog section to integrate the unknown input voltage. After 10,000 internal clocks, the "Sample Control" signal is deactivated and either Ref SW1 or Ref SW2 activates depending upon the comparator logic level. This in turn switches the integrator to the opposite polarity source. Compared to the unknown input voltage, the integrator capacitor is discharged until the output voltage reaches the comparator threshold value. This variable time is proportional to the unknown voltage. The Comparator input voltage change at this time stops the internal counter and internally produces a transfer pulse to store the measured count. The storage registers are fed to the BCD multiplexer which is controlled by a digit select counter. According to the multiplexing sequence, the seven segment information and BCD data are made available at the Seven Segment and BCD Output pins. Note that the Autozero signal is deactivated during the counting cycle. Also, the correct polarity signal Sign Output is available when either of the reference switches are activated.

Transfer Logic and Timing

BCD data in the decade counter is transferred to the storage registers by means of an active Comparator Input. BCD data can also be transferred to the latches under the control of the Transfer input signal.

The Transfer signal at its active (high) state causes a continuous transfer and display mode or it can be pulsed to transfer on command. The Transfer signal in its active state also triggers the auto-range up-down counter whose function is determined by its control logic. The internal transfer pulse is superseded by an external signal applied at the Transfer Input. The Transfer signal in its active state also blanks the Decimal Point Output.

Scan OSC. Logic and Timing

The digit select counter and decoder is edge-triggered from either a signal applied at the Scan OSC. Input or from the output of the internal scan oscillator. The frequency of the internal oscillator is controlled by an RC network tied at this input. The digit select counter is set to the MSD position by a reset signal. Each of the five digit select line outputs is sequentially activated (low) when the corresponding digit is selected. The internal synchronization logic is incorporated to ensure that both the seven segment and BCD data from the selected latch are valid prior to enabling the corresponding Digit Select Output.

Sample/Reset OSC.

An input pulse on this pin activates an internal one-shot which resets the BCD decade counter and forces the digit select counter to the MSD position. This reset pulse also synchronizes the master oscillator frequency to control the logic outputs and BCD counters. An RC network tied to this input causes the internal oscillator to function at the frequency selected.

Leading Zero Blanking and Decimal Point Control

At the start of each MSD to LSD scan cycle, a blanking of leading zeros occurs until the decimal point active state is clocked. Any number following a decimal point is displayed. Leading zero blanking does not affect the BCD outputs and the 10¹ and 10² digits in the display. This feature allows the chip to work as a 3½ DMM. Leading zero blanking is inhibited whenever the Auto Blank Disable is tied to an active (low) level.

Autoranging

The autorange up-down counter is edge triggered by a transfer pulse (internal or external) in conjunction with the associated control logic. The autorange counter is decoded into one of the five output signals through buffers R¹ thru R5. Range R1 acts as R6 when the DP2 control signal is zero.

Down Ranging

If the display count is less than 1800, the autorange counter is downranging, except in the resistance range (Function 2). When in this mode, the counter is upranging. Between count 1800 and 20,000, no autorange movement occurs. At 20,000 or above the counter upranges. Depending upon the state of the Limit 1 and Limit 2 control signals, the scale length could be 20,000, 29,999 or free run.

Flashing Logic

The MSD digit flashes when the count is above 20,000 and the chip is in scale length 29,999 (L2=1,L1=0). If leading zero blanking is not disabled in this mode, all digits except MSD are blanked out and the MSD flashes indicating an overrange situation in the highest possible range. This feature prevents current drain through the segments in an overflow condition.

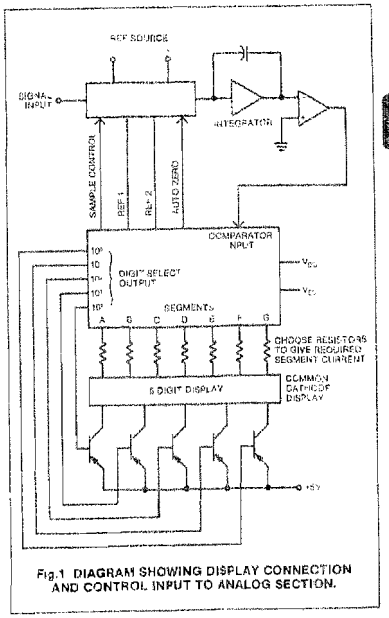
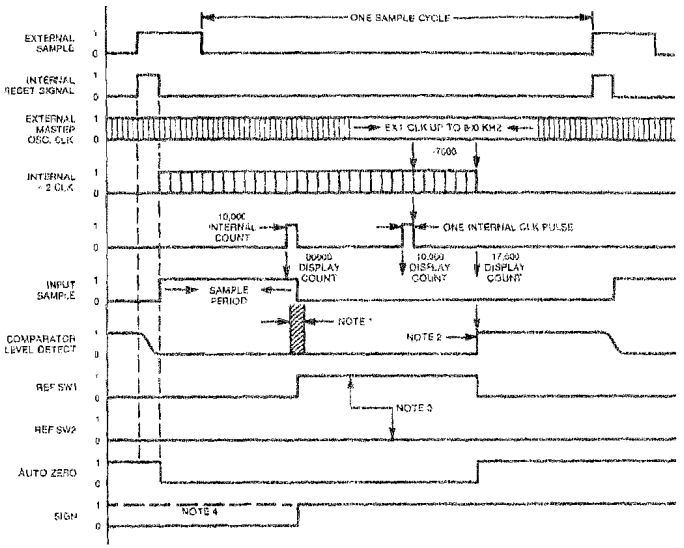


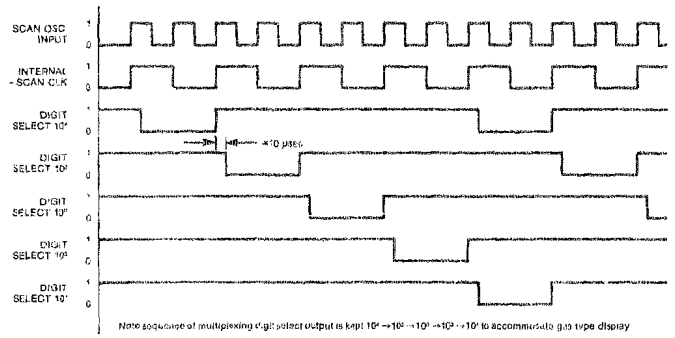
Fig.1 DIAGRAM SHOWING DISPLAY CONNECTION AND CONTROL INPUT TO ANALOG SECTION.

TIMING DIAGRAMS



NOTE
1) During the shaded area, the comparator level DETECT INPUT should be well defined and no noise should be allowed at the input
2) The comparator change is determined by the EXTERNAL CIRCUIT at this point. The count in the counters is proportional to the input measuring voltage
3) The waveform of REF1 and REF2 would be reversed if the comparator level is in the opposite state
4) Polarity would be reversed if the comparator input is reversed

Fig.2 TIMING DIAGRAM OF CONTROL SIGNAL FOR ONE SAMPLE CYCLE



Note sequence of multiplexing digit select output is kept $10^4 \rightarrow 10^3 \rightarrow 10^2 \rightarrow 10^1 \rightarrow 10^0$ to accommodate gas type display

Fig.3 SCAN CLOCK INPUT AND MULTIPLEXING DIGIT SELECT OUTPUT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... +20 to -0.3V
Storage Temperature ..... -55°C to 150°C
Operating Temperature ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below

Standard Conditions (unless otherwise noted)

Operating Temperature (T_A) = 25°C
V_{SS} = 0.0V
V_{DD} = +4.5V to +11V

Parameters	Min	Typ	Max	Units	Conditions
Clocks input voltage low	0.0	—	0.7	V	
Clocks input voltage high					
Pin No. 4,40	V_{DD}-1.0	—	V_{DD}	V	
Pin No. 37	V_{DD}+1.0	—	V_{DD}	V	
Master Clk Freq	DC	(Internal)	400	kHz	From 0°C to 70°C
Scan Clk Freq.	DC	(Internal)	10	kHz	From 0°C to 70°C
Sample Clk Freq.	DC	(Internal)	100	Hz	From 0°C to 70°C
Comparator input voltage HI	3.0	2.8	V_{DD}	V	At V_{DD} = 5V
Comparator input voltage LO	V_{SS}	2.0	2.5	V	At V_{DD} = 5V
Group A					
Input Logic Level HI	V_{DD}-1.0	—	V_{DD}	V	Input Resistance = 100KΩ
Input Logic Level LO	V_{SS}	—	V_{SS}+0.7	V	
Group 2 & 3					
Output Logic Level HI	V_{DD}-1.2	—	V_{DD}	V	At 40μA (V_{DD} = 5V)
Output Logic Level LO	V_{SS}	—	V_{SS}+0.5	V	At 2.0mA
Group 4					
Output Logic Level HI	V_{DD}-1.0	—	V_{DD}	V	At 40μA (V_{DD} = 5V)
Output Logic Level LO	V_{SS}	—	V_{SS}+0.4	V	At 100μA
Group 1					
Output Logic Level HI	V_{DD}-1.2	—	V_{DD}	V	V_{DD} = 5V
Output Logic Level LO	V_{SS}	—	V_{SS}+1.2	V	V_{DD} = 5V @ 1mA
For REF1, REF2, Sample Control, Autozero & Clk Extend					
Output Rise Time	—	—	5.0	μs	V_{DD} = 5V
Output Fall Time	—	—	5.0	μs	
Supply Current	—	—	12	mA	@ V_{DD} = 4V, V_{SS} = 0V, Input Freq = 300 KHz

Pin Numbers

Group A = 15, 16, 17, 25, 26, 38
Group 1 = 3, 5, 6, 7, 8, 9, 23, 28, 29
Group 2 & 3 = 10, 11, 12, 13, 14, 32, 33, 34, 35, 36
Group 4 = 16, 19, 20, 21, 22, 24, 27, 30, 31