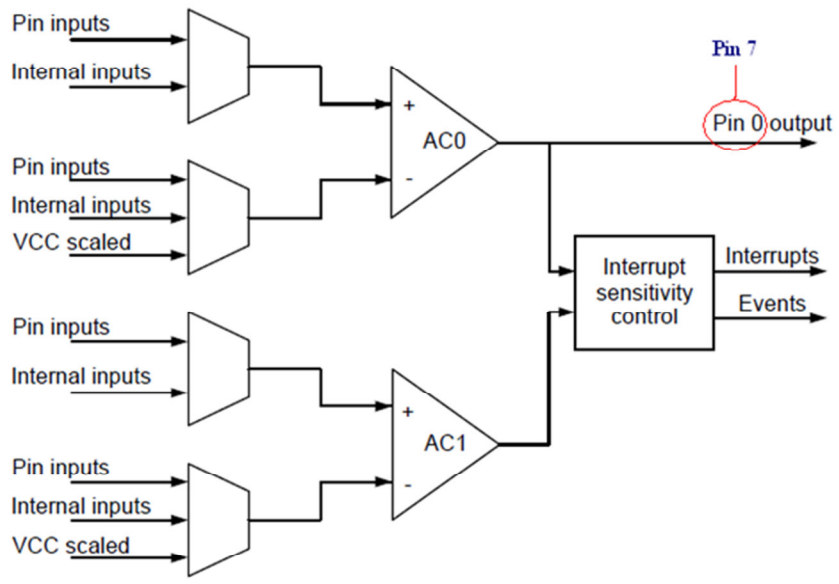
Figure 27-1. Analog Comparator overview.



27.9.3 CTRLA – Control Register A

Bit	7	6	5	4	3	2	1	0	
+0x04	-	-	-	-	-	-	-	AC0OUT	CTRLA
Read/Write	R	R	R	R	R	R	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7:1 - Reserved**

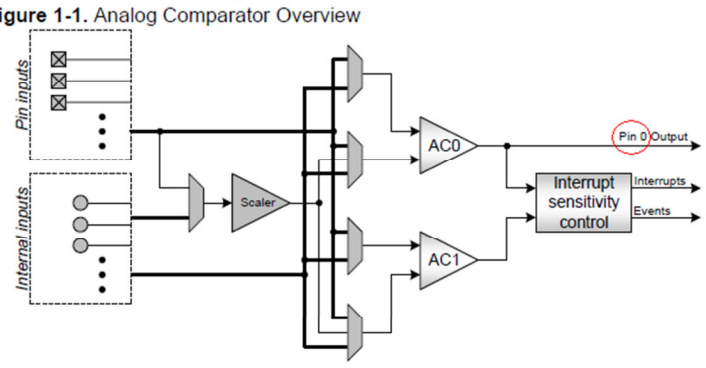
These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.

- **Bit 0 – AC0OUT: Analog Comparator Output**

Setting this bit makes the output of Analog Comparator 0 available on pin 7 on the same port.

27.9.4 CTRLB – Control Register B

Figure 1-1. Analog Comparator Overview



2 Module Overview

This section provides an overview of the basic configuration options and functionality of the Analog Comparator. Section 3 then walks you through the basic steps to get up and running, with register descriptions and configuration details.

2.1 Comparator Operation

Each comparator block has its own set of control and MUX selection registers. For all intents and purposes, they can be operated independently.

In general, if the positive input signal is above the negative input, then the comparator output is logic one, and logic zero otherwise.

Each comparator's *MUX Control* register (`ACnMUXCTRL`) selects the signals to use for the positive and negative input. The positive input can be connected to analog input pin AC0, AC1, AC2, AC4, AC5 or AC6. The negative input can be connected to analog input pin AC0, AC1, AC3, AC5 or AC7.

AC3,