5.3.7.1 Normalization Bit - If the In-Frame Response is employed in the 10.4 Kbps implementation then a "Normalization Bit" is required. The Normalization Bit is described in Paragraph 6.6.2.5.

5.4 Error Detection - The error descriptions in this document are loosely defined and classified. In general, the action taken after an error condition has been detected is manufacturer specific unless it has been specified in this document.

5.4.1 Cyclic Redundancy Check (CRC) - The CRC is required with either of the header byte systems used. The method of calculating and checking the CRC byte is defined below. An invalid CRC byte may constitute a detected error.

a. The CRC calculation and the CRC checker shift registers (or memory locations) will be located in the sender and receiver nodes, respectively, and shall be initially set to the "all ones" state during SOF. (The setting to "ones" prevents an "all zeros" CRC byte with an all zero data stream.)

b. All frame bits that occur after SOF and before the CRC field are used to form the Data Segment Polynomial which is designated as D(X). For any given frame, this number can be interpreted as an "n-bit" binary constant, where n is equal to the frame length, counted in bits.

c. The CRC division polynomial is $X^8 + X^4 + X^3 + X^2 + 1$. This polynomial is designated as P(X).

d. The Remainder Polynomial R(X) is determined from the following Modulo 2 division equation:

Install Equation Editor and double-click here to view equation.

Note: Q(X) is the quotient resulting from the division process.

e. The CRC byte is made equal to $\overline{R(X)}$, where $\overline{R(X)}$ is the ones complement of R(X).

f. The Frame Polynomial M(X) that is transmitted is:

Install Equation Editor and double-click here to view equation.

g. The receiver checking process shifts the entire received frame, including the transmitted CRC byte, through the CRC checker circuit. An error free frame will always result in the unique constant polynomial of $X^7 + X^6 + X^2$ (C4 hex) in the checker shift register regardless of the frame content.

h. Examples of frames with the appropriate CRC bytes are listed in Table 1.

i. A status flag may be used to indicate the occurrence of a received CRC error.

j. When In-Frame Response data is protected by a CRC field, the previous rules are used to define the CRC, except that the sender and receiver nodes are interchanged. The CRC calculation only includes the in-frame response bytes. (Note that the SOF, EOD, EOF, and NB are not used in the CRC calculation and serve as data delimiters.)

TABLE 1 - Examples of Frames & Appropriate CRC Bytes

Data Bytes (hex)	CRC (hex)
00 00 00 00	59
F2 01 83	37
0F AA 00 55	79
00 FF 55 11	B8
33 22 55 AA BB CC DD EE FF	CB
92 6B 55	8C
FF FF FF FF	74

Note: Figure 6 illustrates a typical CRC generator and Figure 7 illustrates a typical CRC checker. With appropriate gating, the two circuits may be combined to use only a single shift register for both CRC generation and CRC checking.